IN THE SPECIFICATION:

Please amend paragraph number **[0006]** as follows:

[0006] Stresses produced in a semiconductor die by application of a layer thereto may be classified as either "intrinsic" or result from "thermal ~~mismatch"between~~ mismatch" between the material of the semiconductor die and the material of the applied layer. In the former case, the applied layer may be in tensile or compressive stress as applied or cured. For example, a polymeric layer may shrink during a curing step to produce intrinsic compressive stress in the active surface of a semiconductor die to which it is attached. Stress resulting from thermal mismatch is particularly evident where the layer deposition is not done at room temperature. Upon cooling to ambient temperature or to a working temperature, different coefficients of expansion (CTE) result in differential contraction or expansion between the semiconductor die substrate, the wafer, and the applied layer. Each of these stress components is important in the fabrication of semiconductor die, particularly where the ratio of semiconductor die thickness to semiconductor die length (or width) is very low.

Please amend paragraph number **[0011]** as follows:

[0011] Conventional laser marking techniques utilize a very high intensity beam of light to alter the surface of a semiconductor die ~~directly~~ by melting, burning, or ablating the device surface directly, or by discoloration or decoloration of a laser reactive coating applied to a surface of the bare semiconductor die or packaged semiconductor die. The beam of light may be scanned over the surface of the bare or packaged semiconductor die in the requisite pattern, or can be directed through a mask which projects the desired inscriptions onto the desired surface of the bare or packaged semiconductor die. The surface or coating of the semiconductor die thus modified, the laser marking creates a reflectivity difference from the rest of the surface of the semiconductor die.v

Please amend paragraph number **[0017]** as follows:

[0017] The present invention provides a method ~~and apparatus~~ for balancing stresses resulting from application of a passivation layer or other layer on the front side of a semiconductor wafer. The term "passivation layer" will be used herein to denote any front side layer (compressive or tensile) which creates stress in the singulated die tending to form warp. The method and apparatus have particular application to wafers or semiconductor die which have been subjected to a thinning process, including backgrinding in particular. The present method comprises application of a stress-balancing layer (SBL) on the opposite side from a ~~stress-creating~~ stress-creating layer such as a photoresist passivation layer, for example. Thus, a passivation layer covering the circuitry of each semiconductor die of a wafer will typically introduce compressive stresses into the dice; a stress-balancing layer (SBL) which is applied after wafer thinning but before singulation will result in individual semiconductor die in which the front side stresses and back side stresses are balanced, preventing dice warp.

Please amend paragraph number **[0033]** as follows:

[0033] FIG. 8 is a cross-sectional view of a wafer following application of a ~~stress-balancing~~ stress-balancing layer on the thinned back side thereof;

Please amend paragraph number **[0046]** as follows:

[0046] Turning now to FIG. 2A, a side cross-sectional view of a prior art semiconductor die 20A having a thickness ~~92 is~~ 42 is shown with a passivation layer 40A having a thickness 44 joined to the front side 11. Some features are exaggerated for the sake of clarity. The passivation layer 40A is shown as having laterally "shrunk" relative to the semiconductor die 20A at the extant temperature, resulting in compressive lateral stress ~~forces16~~ forces 16 acting at the ~~die-layer~~ die-layer interface 22. Reactive stress forces 18 in the semiconductor die 20A oppose the applied stress forces ~~forces~~ 16, and the stress forces 16, 18 result in what is denoted herein as compressive warp.

Please amend paragraph number **[0047]** as follows:

[0047] As shown in FIG. 2B, semiconductor die 20B ~~of the~~ of a prior art is shown with passivation layer 40B joined to the front side 11. The passivation layer 40B has laterally "expanded" relative to the semiconductor die 20B, creating tensile lateral stress forces 16 acting at the die-layer interface 22. Reactive stress forces 18 in semiconductor die 20B oppose the applied stress forces 16, and the result is what is denoted herein as tensile warp.

Please amend paragraph number **[0048]** as follows:

[0048] The degree of warp, whether compressive or tensile, depends upon the aspect ratio of the semiconductor die 20 and the active stress forces 16, 18. Minimization or elimination of die warp is important to the manufacture of a high quality ~~dice~~ die with a minimum number of defects.

Please amend paragraph number **[0050]** as follows:

[0050] A portion of a semiconductor wafer 10 is depicted in FIG. 3 as comprising a wafer substrate 32. The wafer 10 has a front side 11, an opposing back side 12, and a circumferential edge 28. The wafer ~~is~~ 10 is sliced from a crystalline cylinder of a semiconductive material such as silicon, germanium, gallium arsenide, etc. which comprises the wafer substrate 32.

Please amend paragraph number **[0053]** as follows:

[0053] Referring now to FIG. 6, it is seen that an electrically insulative passivation layer 40 is typically applied to cover the microcircuit 30 following circuit fabrication. The passivation layer 40 protects the microcircuit 30 from damage during subsequent manufacturing steps as well as in ultimate use. Unprotected, the microcircuit 30 may be degraded by contamination, chemical action, corrosion, and/or handling. Passivation layer 40 may comprise any of a variety of materials, including silicon dioxide and silicon nitride as examples. Such materials are typically applied by a chemical vapor deposition (CVP) process at elevated

temperature. Thus, a difference in coefficient of thermal expansion (CTE) between the passivation layer 40 and the die material to which it is applied will result in a residual stress in the wafer 10, and in semiconductor dice 20 when the wafer ~~is~~ 10 is diced (die singulation). For example, silicon has a CTE which is several times the CTE of silicon dioxide and will contract much more than a silicon dioxide passivation layer upon cooling from an elevated temperature, creating stress which is concentrated at the die-layer interface 22 between the wafer 10 and the passivation layer 40.

Please amend paragraph number **[0054]** as follows:

[0054] As depicted in FIG. 7, the back side 12 of the wafer 10 is then ground to reduce the wafer thickness 42 of the wafer substrate 32. In a conventional back-grinding process, illustrated in FIG. 11, a grinding wheel 52 with grinding surface 53 grinds away a portion 25 (see FIG. 7) of semiconductor wafer substrate ~~material~~ 32 from the back side ~~surface~~ 12. Such grinding to fully thin the wafer thickness 42 typically leaves a somewhat nonsmooth ground surface 24 with grooves and/or swirls present. However, the unevenness makes the ground surface 24 conducive to later adhesive attachment of a stress-balancing layer 50 (FIG. 8) thereto.

Please amend paragraph number **[0057]** as follows:

[0057] The stress-balancing layer 50 may be formed in a variety of ways. For example, the SBL 50 may comprise a single rigid layer or a multifilm layer with each layer formed to resist deformation in a different direction, or with different deformation properties. In another form, homogeneously distributed inorganic particles may be bound in a matrix for uniform stress resistance in an X-Y plane, or optionally, omnidirectional. The stress-balancing layer 50 may be formed of any material or materials which when applied in a thin layer to the back side semiconductor die ~~guard~~ ground surface 24, will provide a rigid structure resistant to warping of the semiconductor die 20.

Please amend paragraph number **[0061]** as follows:

[0061] In a further embodiment shown in FIG. 14, two or more layers of composite materials (depicted as 50A and 50B) are sequentially deposited as a stress-balancing layer 50. Each layer is shown with a reinforcing material 74A or 74B configured to resist stresses (i.e., have highest rigidity) in a particular direction, so that the layer combination provides the desired warping resistance.

Please amend paragraph number **[0063]** as follows:

[0063] The SBL 50 may itself comprise an adhesive material, particularly when combined with added reinforcement particles. For example, polymeric materials known in the art may be applied to form a rigid structure, yet retain adhesive properties. Thus, semiconductor dice 20 formed therefrom may be adhesively attached to a circuit board or other substrate.

Please amend paragraph number **[0064]** as follows:

[0064] In an alternative embodiment of the present invention, an adhesive layer 48 may be applied to the stress-balancing layer 50, as depicted in FIG. 15. The adhesive layer 48 may be formed of a type of adhesive material characterized as being epoxy, or other suitable adhesive material. This adhesive layer 48 may be used as a die attach adhesive, or may be used to temporarily attach a carrier tape 62 to the wafer 10, as in FIG. 16. As discussed, infra, the adhesive layer 48 may also comprise a markable material such as a UV acrylic, thio-phene,~~ poly-paraxylylene,~~ poly-paraxylylene (Paralene), urethanes, silicones, and acrylics, provided its strength is sufficient to resist die warping. Carrier tapes 62 are generally used to protect and hold the semiconductor dice 20 in place during sawing of the wafer 10 and enable convenient pick-off of individual semiconductor die 20 for transfer to a substrate in a semiconductor die 20 attach step.

Please amend paragraph number **[0065]** as follows:

[0065] Another embodiment of the invention utilizes a tape as a stress-balancing layer 50, wherein stresses in the plane of the tape are resisted by rigidity. The tape may be monolayer or multilayer and may be formed of or include a metal film. It is important to utilize an adhesive which will rigidly adhere to the tape and semiconductor die 20 as a very thin film. The tape may be thinly adhesed on both sides, for temporary attachment to a carrier tape 62 or for permanent semiconductor die attach to a circuit board or other substrate, not shown in the figures.

Please amend paragraph number **[0066]** as follows:

[0066] Whether the stress-balancing layer 50 is applied as a tape or as a CVD layer, it may be applied to overcover the entire thinned ground surface 24, or alternatively cover selected portions of the wafer 10 or of each semiconductor die 20. For example, as shown in FIG. 18, an SBL 50 may be applied in various patterns of stress-balancing layers 50X, 50Y and 50Z on the thinned semiconductor die back side 12 of each semiconductor die 20 of a wafer 10. As shown in these examples,~~stress-balancing~~ stress-balancing layer 50X is configured to cover the entire back side 12 as a contiguous layer. In another embodiment, the stress-balancing layer 50Y may be patterned, for example, as a continuous longitudinal strip extending over a row of semiconductor dice 20. In a further variation, stress-balancing layers 50Z are shown as discrete coverings for each individual semiconductor~~die.~~ die 20. The SBL 50Z is shown as comprising a rectangular covering over a majority of a semiconductor die back side 12. However, it may comprise any pattern 68 which achieves the desired stress balancing. If applied as a tape, stress-balancing layer 50 may be applied by an automated process such that the tape is in a highly regular and standard pattern corresponding to placement on predetermined specific areas on the semiconductor dice 20, or on wafer areas which will correspond to individual semiconductor dice after singulation. As such, vision systems for reading marks on semiconductor dice can be

adjusted to scan the desired marked areas. In the view of FIG. 18, the outer surface 36 of the stress-balancing ~~layer~~ layers 50X, 50Y or 50Z is uniformly planar for subsequent semiconductor die attach.

Please amend paragraph number **[0067]** as follows:

[0067] Although the stress-balancing layer 50 may be sometimes usefully applied to already singulated semiconductor die 20, it is preferred to apply stress-balancing layer 50 to the wafer ground surface 24 prior to singulation, because this avoids warpage resulting from singulation and is generally more cost-effective.

Please amend paragraph number **[0068]** as follows:

[0068] Exemplary semiconductor dice 20C and 20D formed by the method of the invention are illustrated in FIGS. 17A and 17B. As illustrated in FIG. 17A and 17B, a ~~stress-balancing~~ stress-balancing layer 50C or 50D is applied to the back side 12 of a semiconductor die 20C, 20D, respectively. This stress-balancing layer 50C or 50D balances reactive stress forces 18 in semiconductor die 20C or 20D caused by compressive or tensile stress forces 16 in passivation ~~layer~~ layers 40C and 40D, and maintain the semiconductor dice in a generally warp-free condition. The counter forces 70 in the SBL 50C, 50D balance the warping stress forces 16 in the passivation ~~layer~~ layers 40C, 40D.

Please amend paragraph number **[0069]** as follows:

[0069] The SBL 50 is particularly useful when it, or an adhesive layer 48 applied thereto, is configured to be used as an indicia marking layer. FIG. 19 illustrates in a simplified schematic view of a conventional laser marking system 100 capable of readily marking semiconductor dice 20 to which a laser markable material has been applied. The system 100 comprises a laser 102, a lens system 104, a shadow mask 106 and a laser control system 108 for monitoring and controlling the function of the apparatus. For purposes of this invention, a "laser" is considered to be any optical energy source capable of marking a surface of a ~~stress-~~

~~balancing~~ stress-balancing layer 50 through the use of light energy and/or heat. Preferably, laser 102 is comprised of an Nd:YAG (yttrium aluminum garnet), Nd:YLP (pulsed yttrium fiber laser), carbon dioxide, or other suitable optical energy devices known in the art. It is understood, however, that laser 102 may also comprise an ultraviolet (UV) energy source or other energy beam. When laser 102 is energized, an intense beam of light 115 is projected from lens system 104 through shadow mask 106 onto the surface of the laser-markable material (SBL 50 or adhesive layer 48 applied thereto). When laser beam 115 impinges on laser markable material ~~50,~~ SBL 50 or adhesive layer 48, the material in, on, embedded in, attached to or under the material is altered, e.g., by heating, vaporization, burning, melting, chemical reaction, residue or dye transfer, or combinations thereof. The result comprises a color or texture change, or both, having an image of shadow mask 106 appearing on the ground surface 24 of the semiconductor die 20. Although a shadow mask 106 is shown in this embodiment, the present invention contemplates computer-directed operation, including mechanical movement of laser 102 in conjunction with, or without, shadow mask 106.

Please amend paragraph number **[0072]** as follows:

[0072] Thus, in the present invention, a stress-balancing layer 50 may be formed on the ground surface 24 of a semiconductor wafer 10 to balance warping stresses in the subsequently singulated semiconductor dice 20. In addition, the stress-balancing layer 50 may be configured to be or support a markable layer on the die's thinned ground surface 24. The stress-balancing layer 50 may also be configured to comprise or support a semiconductor die attach adhesive or carrier adhesive.

Please amend paragraph number **[0073]** as follows:

[0073] The stress-balancing layer 50 which is applied to the back side 12, ground surface 24 of a thinned wafer 10 may comprise only a very small portion of the Z dimension of the subsequently singulated dice. The wafer thickness 42 of the SBL 50 will depend upon the footprint size and thickness of the die and will generally be larger as the footprint increases.

Typically, for the stresses normally encountered in small semiconductor dice 20, i.e., less than about 10 mm in the X and Y dimensions and less than about 1.5 mm in the Z dimension, the wafer thickness 42 of the SBL 50 is generally less than about 0.1 mm and effectively prevents or counteracts the tendency to warp. The SBL 50 may be formed of the same material as the stress-causing passivation layer 40 and be of a similar wafer thickness 42.